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A New Triple-Switch-Triple-Mode High Step-Up Converter with Wide Range of Duty Cycle for DC Microgrid Applications

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***Abstract*—DC microgrid is gaining attraction and a recent trend in distribution power generation system due to penetration of renewables (especially Photovoltaic (PV) or Fuel Cell (FC)). In this paper, a new Triple-Switch-Triple-Mode High Step-Up converter (TSTM-HS converter) is presented for DC microgrid applications. In the proposed converter, voltage lift technique is employed and range of duty cycle is extended by incorporating an additional switch in converter circuitry. By doing this, high voltage conversion ratio is achieved without using a transformer, coupled inductor, and multiple stages of switched capacitors. Moreover, the TSTM-HS converter operated in three modes with two types of the duty cycles to achieve low to high voltage conversion without using high duty cycle for each switch. The effects of difference in the inductance values on the regulation and operating behavior of the TSTM-HS converter are discussed. The Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) characteristics of TSTM-HS converter are discussed in detail with steady-state analysis and boundary condition. The comparison is provided to highlight the benefits of the TSTM-HS converter. The selection of semiconductor devices and the design of reactive components are discussed for the TSTM-HS converter. The experimental results of the proposed converter are provided which validate the theoretical approach, performance, and feasibility of converter.**

***Index Terms*— DC-DC converter, DC microgrid, High voltage conversion ratio, Triple-Switch-Triple-Mode converter, Voltage-lift, Wide range of duty cycle.**

I. Introduction

DC microgrid and its associated power electronics converter units are the main attraction and rapidly upgrading technologies due to penetration of renewables in the distribution power generation energy systems. Photovoltaic (PV), Fuel Cell (FC), and batteries are mainly employed to powered DC microgrid via power conversion unit [1]-[2]. Several PV or FC sources can also be connected in series or parallel for the generation of the high DC voltage and current. However, several sources in series or parallel for the energy generation is not a viable solution to fulfil the voltage and current demand of load due to the requirement of higher cost and large space for the installation etc. Therefore, DC-DC converter is generally employed as a front-end structure to achieve high voltage or high current with high efficiency and small volume [3]-[5]. Fig. 1 depicts the structure of 400V DC microgrid system in which high voltage is obtained with the help of DC-DC converter from 12-48V PV sources. Theoretically, the conventional converter provides higher voltage conversion ratio at higher duty cycle. However, in practical, due to use of extreme duty cycle, the performance and efficiency of the conventional DC-DC boost converter are highly suffered from the diode reverse recovery problem, Effective Series Resistance (ESR) of inductor and capacitor, electromagnetic interference, and conduction losses of switches [6]-[7]. Isolated converter configurations e.g. push-pull, flyback, forward, half-bridge, and full-bridge converters has been proposed in the literature to achieve high voltage conversion by adjusting the turn ratio of the transformer or coupled inductors [8]-[10]. Nevertheless, transformer core saturation, high voltage spikes across switches, power dissipation, bulky circuitry etc. are the main problem associated with these configurations. Moreover, an additional active clamping circuit, a non-dissipative snubber circuit, and high-frequency transformer are required which increases the cost and size of the converter [11]-[12].

The non-isolated converter can be a viable solution to achieve high voltage conversion ratio in case galvanic isolation is not required [13]-[14]. Several converter configurations are also presented in the literature by utilizing the coupled inductor to achieve high voltage conversion ratio [15]-[16]. However, high input current ripples, voltage spikes on the switch, and leakage inductance are the main problems associated with these configurations. Therefore, an additional

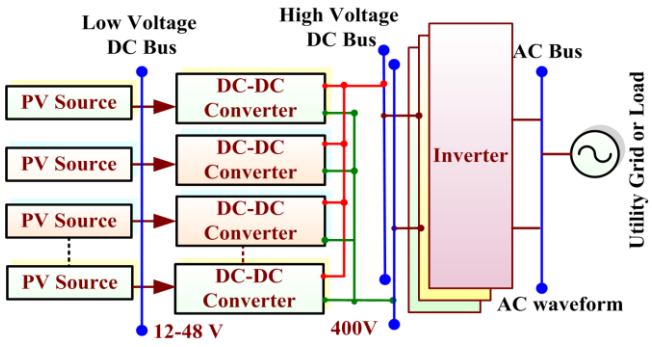

Fig. 1. Block diagram of 400V DC microgrid system for with PV.

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input filter and active clamping techniques are needed for coupled inductor based power converters [17]. Several converter configurations have been addressed based on the multiple boosting stages without using transformer and coupled inductors e.g. cascaded and quadratic boost, voltage lift technique, Voltage Multiplier (VM), Switched Capacitor (SC), integration of boost converter with SC, Switched Inductor (SI) [18]-[22]. The insertion of a large number of multiple stages with inductors and capacitors surely increases the complexity and cost of the power circuit. In SC technique, multiple capacitors stages are required and the switches are suffered from the high transient current and high conduction losses. In [23], the power circuitries of three converters are proposed to achieve higher voltage conversion in which two inductors are charged in parallel and discharged in series when the switches are turned ON and OFF, respectively. In [24], several numbers of diode-capacitor stages are employed to achieve higher voltage conversion ratio. The multiple loops to transfer the energy to load degrade the efficiency and circuitry also required inductor with high current capability. Moreover, the converter has a narrow range of duty cycle for the switching operation. In [25], high gain converter is proposed for microgrid applications by incorporating additional switch. However, the conversion ratio is not significantly increased even using three switches. In [26], a new converter is proposed by using several inductors and switches. However, utilization of several switched inductors is not a viable solution and moreover, a large number of semiconductor devices are required to transfer energy to load via inductors. As a result, cost and size of the converter is increased. In this paper, a new converter called Triple-Switch-Triple-Mode High Step-Up converter (TSTM-HS converter) is proposed to overcome the aforementioned drawbacks. The TSTM-HS converter has the capability to generate higher voltage conversion ratio with a wide range of duty cycle. The other advantages of the TSTM-HS converter are output voltage is achieved by adjusting the two types of the duty cycle, transformer-less configuration, coupled inductor-less configuration, the stored energy is supplied to load without using a large number of semiconductor devices, and high voltage conversion ratio without using VM.

The paper is organized as follows: power circuitry, operating principle of the TSTM-HS converter along with CCM and DCM analysis and characteristics are discussed in section II. The effects of difference in the inductance values on the regulation and operation of the TSTM-HS converter are discussed in Section III. The efficiency analysis of the converter is discussed in section IV. The design of TSTM-HS converter is provided in section V. Also, the TSTM-HS converter compared with recently presented converter to show the benefits of the proposed approach. The experimental results are provided in the section VI. Finally, a conclusion based on the experimental investigation is provided in section VII. References are given in the last section to support the literature and concept of the proposed converter.

II. Triple-Switch-Triple-Mode High Step-Up Converter (TSTM-HS Converter)

Fig. 2 shows the power circuitry of TSTM-HS converter. The circuitry consists of two inductors L_1 and L_2; two control switches S_1 and S_2 (bidirectional for current); switch S_3 (diode D is connected in series to achieve unidirectional current), three capacitors C_1, C_2, and C_o; three diodes D_1, D_2, and D_o. The load R is connected across capacitor C_o. The inductance level for both the inductors L_1 and L_2 are same; hence, $L_1=L_2=L$. The capacitance of both capacitor C_1 and C_2 are same; hence, $C_1=C_2=C$. In this section, it is assumed that inductance values of both inductors are equal i.e $L_1=L_2=L$. Therefore, this section deals with CCM and DCM characteristics by considering $L_1=L_2=L$. However, in practical

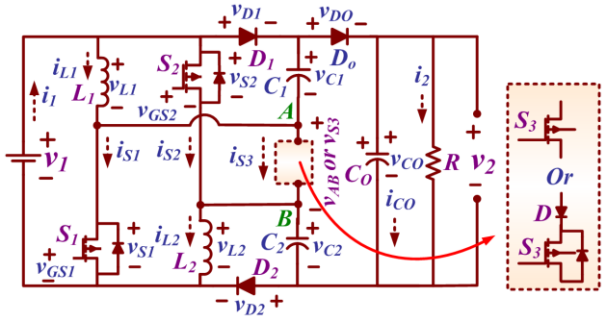

Fig. 2. Power circuitry of TSTM-HS converter.

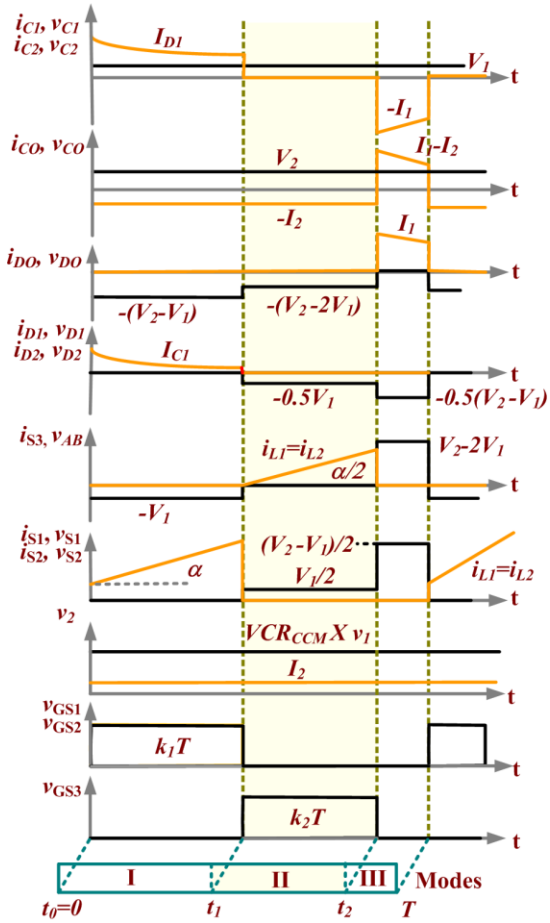

Fig. 3. Typical characteristics waveform of CCM.

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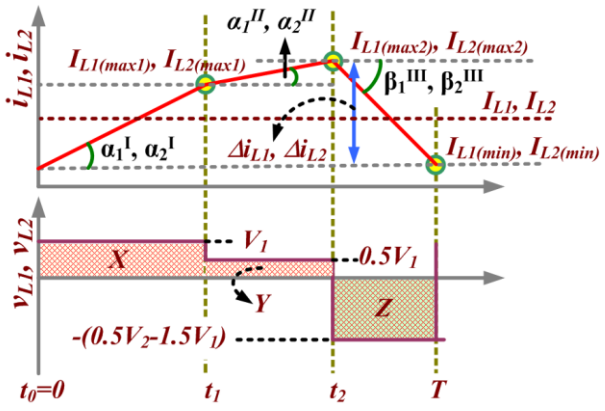

Fig. 4. Inductor voltage and current waveform.

cases, the converter operating behavior and regulation surely affect by the difference in the two inductances values i.e. L_1 and L_2 which is discussed in section III.

To elucidate the CCM and DCM operation of TSTM-HS converter, steady state analysis and characteristic, it is assumed that all the reactive components and semiconductor devices are ideal, (i.e. ON-state resistance ($R_{D\text{-}ON}$) of semiconductor devices and voltage drop during conduction are zero), ESR of all the inductors and capacitors are zero, and all the capacitors have enough capacitance to provide ripple free voltage (i.e. ΔV_{C1}, ΔV_{C2}, and ΔV_{C3} are zero). Let's assumes T and f_s is time period of one switching cycle and switching frequency, respectively.

A. CCM- Characteristics Waveform, Operation, and Analysis

The gate pulses are provided to three switches S_1, S_2, and S_3 in such a way that the circuitry of converter performs three modes of operation in CCM. The gate pulses for switches S_1 and S_2 are identical with duty ratio k_1, and the gate pulse with duty ratio k_2 is provided to switch S_3 with delay k_1T seconds. The typical characteristics waveform of CCM is shown in Fig. 3. The inductor voltage and current waveform is separately shown in Fig. 4, where α_1^I, α_2^I, α_1^{II}, and α_2^{II} are magnetizing angle, and β_1^{III}, β_2^{III} are demagnetizing angle for inductors L_1, L_2 for modes I, II, and III, respectively (where superscript denotes the mode and subscript denotes the inductor). The magnetizing angle is angle measured between charging current of inductors and time axis. Similarly, the demagnetizing angle is angle measure between discharging current of inductors and time axis. The X, Y, and Z are regions trace by voltage of inductors L_1 and L_2 in mode I, II, and III, respectively. The operating principle and analysis of converter for each mode is explains as follows,

1) Mode I [t_0-t_1]: For this mode, switches S_1 and S_2 are turned ON, and switch S_3 is turned OFF. Fig. 5(a) depicts the equivalent converter circuitry for this mode. During this mode, inductors L_1, L_2, and capacitors C_1, C_2 are connected in parallel with input supply v_1. Therefore, both inductors L_1 and L_2 are magnetized by input supply voltage (v_1) through the path v_1-L_1-S_1 and v_1-S_2-L_2, respectively. At the same time,

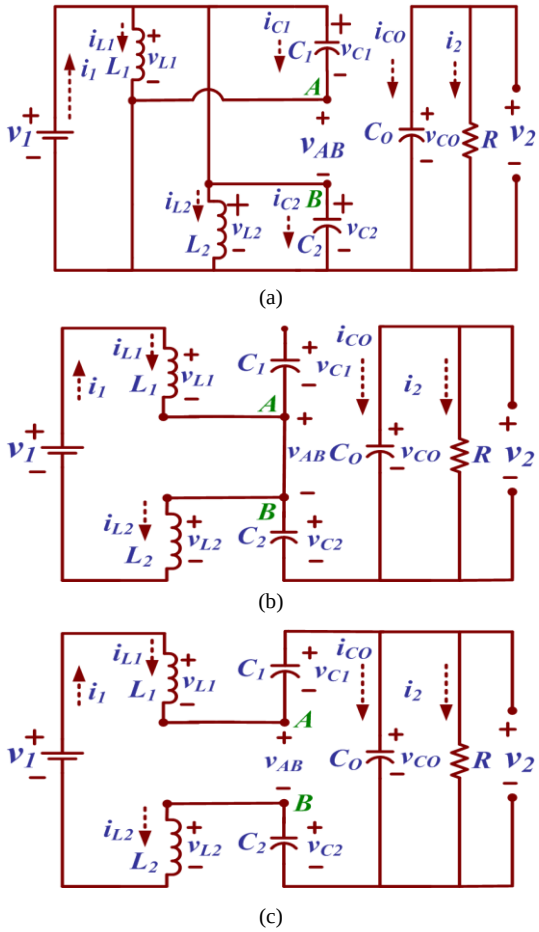

Fig. 5. Equivalent circuitry (a) when switches S_1 and S_2 are turned ON, and switch S_3 is turned OFF, (b) switches S_1 and S_2 are turned OFF, and switch S_3 is turned ON, (c) all switches S_1, S_2, and S_3 are turned OFF.

capacitors C_1 and C_2 are also charged by input voltage (v_1) through the path v_1-D_1-C_1-S_1 and v_1-S_2-C_2-D_2, respectively. The load R is continuously supplied by the energy stored in the capacitor C_o. Diodes D_1 and D_2 are forward biased and diode D_o is reversed biased. From the equivalent circuitry and characteristics, the voltage across inductors and capacitors are expressed as follows,

$$v_{L1} = v_{L2} = v_L \approx V_1;\ V_{C1} = V_{C2} = V_C \approx V_1;\ V_{Co} \approx V_2 \qquad (1)$$

In this mode, inductors L_1 and L_2 currents are linearly increasing with constant slope tan α_1^I and tan α_2^I, respectively. The magnetizing angle of inductors L_1 and L_2 (α_1^I and α_2^I) can be expressed as follows,

$$\left.\begin{aligned} \alpha_1^I &= \tan^{-1}\left(\frac{V_1}{L_1}\right) = \tan^{-1}\left(\frac{I_{L1(max1)} - I_{L1(min)}}{k_1 T}\right) \\ \alpha_2^I &= \tan^{-1}\left(\frac{V_1}{L_2}\right) = \tan^{-1}\left(\frac{I_{L2(max1)} - I_{L2(min)}}{k_1 T}\right) \\ &\text{we have } L_1 = L_2,\ \therefore \tan\alpha_1^I = \tan\alpha_2^I \Rightarrow \alpha_1^I = \alpha_2^I = \alpha \end{aligned}\right\} t_0 \le t \le t_1 \qquad (2)$$

2) Mode II [t_1-t_2]: For this mode, switches S_1 and S_2 are turned OFF, and switch S_3 is turned ON. Fig. 5(b) depicts the equivalent converter circuitry for this mode. During this mode, inductors L_1 and L_2 serially connected with input supply.

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Therefore, series network of inductors L_1 and L_2 are magnetized by input supply voltage (v_1) through the path v_1-L_1-S_3-L_2, respectively. The voltage across capacitors C_1, C_2, and C_o incurs the diodes D_1, D_2 and D_o in reversed biased operation. Due to this, energy stored in capacitors C_1 and C_2 are unchanged and the load R is yet supplied by energy stored in the capacitor C_o. From the equivalent circuitry and characteristics, the voltage across inductors and capacitors are expressed as follows,

$$v_{L1} = v_{L2} = v_L \approx \frac{V_1}{2};\ V_{C1} = V_{C2} = V_C \approx V_1;\ V_{Co} \approx V_2 \tag{3}$$

In this mode, inductors L_1 and L_2 currents are linearly increasing with constant slope tan α_1^{II} and tan α_2^{II}, respectively. The magnetizing angle of inductors L_1 and L_2 (α_1^{II} and α_2^{II}) can be expressed as follows,

$$\left.\begin{aligned} \alpha_1^{II} &= \tan^{-1}\left(\frac{V_1}{2L_1}\right) = \tan^{-1}\left(\frac{I_{L1(max2)} - I_{L1(max1)}}{k_2 T}\right) \\ \alpha_2^{II} &= \tan^{-1}\left(\frac{V_1}{2L_2}\right) = \tan^{-1}\left(\frac{I_{L2(max2)} - I_{L2(max1)}}{k_2 T}\right) \\ \text{we have } L_1 = L_2,\ \therefore\ &\tan\alpha_1^{II} = \tan\alpha_2^{II} \Rightarrow \alpha_1^{II} = \alpha_2^{II} = \alpha/2 \end{aligned}\right\} t_1 \le t \le t_2 \tag{4}$$

3) Mode III [t_2-t_3]: For this mode, all switches S_1, S_2, and S_3 are turned OFF. Fig. 5(c) depicts the equivalent converter circuitry for this mode. During this mode, inductors L_1 and L_2 along with capacitors C_1 and C_2 are serially connected with input supply and supplied energy to capacitor C_o and load R. Thus, inductors L_1 and L_2 demagnetized and capacitor C_1 and C_2 are discharged through the path v_1-L_1-C_1-R-C_2-L_2. Diodes D_1 and D_2 are reversed biased and diode D_o in forward biased. From the equivalent circuitry and characteristics, the voltage across inductors and capacitors are expressed as follows,

$$\left.\begin{aligned} v_{L1} = v_{L2} = v_L &= \frac{V_1 + V_{C1} + V_{C2} - V_2}{2} \approx \frac{3V_1 - V_2}{2} \\ V_{C1} = V_{C2} = V_C &\approx V_1;\ V_{Co} \approx V_2 \end{aligned}\right\} \tag{5}$$

In this mode, inductors L_1 and L_2 currents are linearly decreasing with constant slope tan β_1^{III} and tan β_2^{III}, respectively. The demagnetizing angle of the inductors L_1 and L_2 (β_1^{III} and β_2^{III}) can be expressed as follows,

$$\left.\begin{aligned} \beta_1^{III} &= \tan^{-1}\left(\frac{3V_1 - V_2}{2L_1}\right) = \tan^{-1}\left(\frac{I_{L1(min)} - I_{L1(max2)}}{1 - k_1 T - k_2 T}\right) \\ \beta_2^{III} &= \tan^{-1}\left(\frac{3V_1 - V_2}{2L_2}\right) = \tan^{-1}\left(\frac{I_{L2(min)} - I_{L2(max2)}}{1 - k_1 T - k_2 T}\right) \\ \text{we have } L_1 = L_2,\ \therefore\ &\tan\beta_1^{II} = \tan\beta_2^{II} \Rightarrow \beta_1^{II} = \beta_2^{II} = \beta \end{aligned}\right\} t_2 \le t \le T \tag{6}$$

Using inductor volt-second balance method,

$$\underbrace{\int_0^{k_1 T} v_L^{I}\, dt}_{X} + \underbrace{\int_0^{k_2 T} v_L^{II}\, dt}_{Y} + \underbrace{\int_0^{1-k_1 T-k_2 T} v_L^{III}\, dt}_{Z} = 0 \tag{7}$$

Where, v_L^{I}, v_L^{II}, and v_L^{III} are voltage across inductors in mode I, II, and III, respectively. X, Y, and Z are the area trace under inductors voltage waveform as shown in Fig. 4. Using (7), the voltage conversion ratio for CCM (VCR_{CCM}) of the TSTM-HS converter is obtained as follows,

$$\int_0^{k_1 T} (V_1)\, dt + \int_0^{k_2 T} \left(\frac{V_1}{2}\right) dt + \int_0^{1-k_1 T-K_2 T} \left(\frac{3V_1 - V_2}{2}\right) dt = 0 \tag{8}$$

$$VCR_{CCM} = \frac{V_2}{V_1} = \frac{3 - k_1 - 2k_2}{1 - k_1 - k_2} \tag{9}$$

The effects of duty cycles k_1 and k_2 on voltage conversion ratio are analyzed. The variation in the voltage conversion

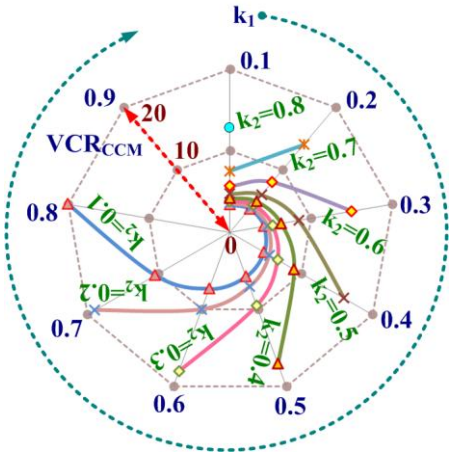

Fig. 6. Plot of voltage conversion ratio and effect of k_1 and k_2 on voltage conversion ratio.

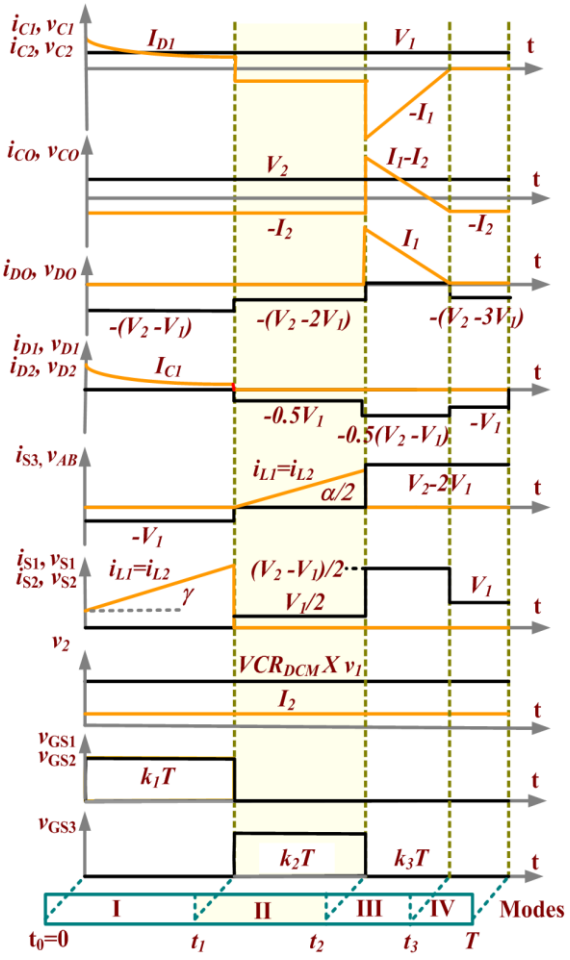

Fig. 7. Typical characteristics waveform of DCM.

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ratio VCR_{CCM} with change in duty cycle k_1 and keeping k_2 constant, and the variation in the voltage conversion ratio VCR_{CCM} with change in duty cycle k_2 and keeping k_1 constant is shown in Fig. 6. It is investigated that the TSTM-HS converter provides a high voltage conversion ratio by varying duty cycle suitably.

B. DCM- Characteristics Waveform, Operation, and Analysis

For DCM, operation of the TSTM-HS converter is divided in four modes. The typical characteristics waveform is shown in Fig. 7, voltage and current waveform of inductors L_1 and L_2 are separately shown in Fig. 8, where δ_1^I, δ_2^I; δ_1^{II}, and δ_2^{II} are magnetizing angles and γ_1^{III}, γ_2^{III} are demagnetizing angles for inductors L_1 and L_2 for mode I, II, and III, respectively (where superscript denotes the mode and subscript denotes the inductor). The X, Y, Z, U are regions trace by voltage of inductors L_1 and L_2 in mode I, II, III, and IV, respectively. The modes are explained as follows,

1) Mode I [t_0-t_1]: For this mode, switches S_1 and S_2 are turned ON, and switch S_3 is turned OFF. For this mode, operating principle and equivalent circuitry (Fig. 5(a)) are same as mode I of CCM. The maximum value of inductors L_1 and L_2 currents are expressed as follows,

$$\left.\begin{aligned} &I_{L1(max1)}=\left(\frac{V_1}{L_1}\right)k_1T=k_1T\tan(\delta_1{}^I)\\ &I_{L2(max1)}=\left(\frac{V_1}{L_2}\right)k_1T=k_1T\tan(\delta_2{}^I)\\ &\text{we have } L_1=L_2=L,\\ &\therefore I_{L1(max1)}=I_{L2(max1)}=I_{L(max1)}\Rightarrow\delta_1{}^I=\delta_2{}^I=\delta \end{aligned}\right\} t_0\le t\le t_1 \quad (10)$$

2) Mode II [t_1-t_2]: For this mode, switches S_1 and S_2 are turned OFF, switch S_3 is turned ON, and inductors L_1 and L_2 currents are non zero. For this mode, operating principle and equivalent circuitry (Fig. 5(b)) are same as mode II of CCM. The maximum value of inductor L_1 and L_2 currents is expressed as follows,

$$\left.\begin{aligned} &I_{L1(max2)}\begin{cases}=I_{L1(max1)}+\left(\frac{V_1}{2L_1}\right)k_2T\\ =\left(\frac{V_1}{L_1}\right)\left(\frac{k_2T}{2}+k_1T\right)\\ =k_2T\tan(\delta_1{}^{II})+k_1T\tan(\delta_1{}^I)\end{cases}\\ &I_{L2(max2)}\begin{cases}=I_{L2(max1)}+\left(\frac{V_1}{2L_2}\right)k_2T\\ =\left(\frac{V_1}{L_2}\right)\left(\frac{k_2T}{2}+k_1T\right)\\ =k_2T\tan(\delta_2{}^{II})+k_1T\tan(\delta_2{}^I)\end{cases}\\ &\text{we have } L_1=L_2=L,\Rightarrow\delta_1{}^{II}=\delta_2{}^{II}=\frac{\delta_1^I}{2}=\frac{\delta_2{}^I}{2}=\frac{\delta}{2}\\ &\therefore I_{L1(max2)}=I_{L2(max2)}=I_{L(max2)} \end{aligned}\right\} t_1\le t\le t_2 \quad (11)$$

3) Mode III [t_2-t_3]: For this mode, all the switches S_1, S_2, and S_3 are turned OFF, and inductors L_1 and L_2 currents are non zero. For this mode, operating principle and equivalent circuitry (Fig. 5(c)) are same as mode III of CCM. The value of inductors L_1 and L_2 currents are reached to zero at time t_3, and the maximum value of inductors L_1 and L_2 currents can be expressed as follows,

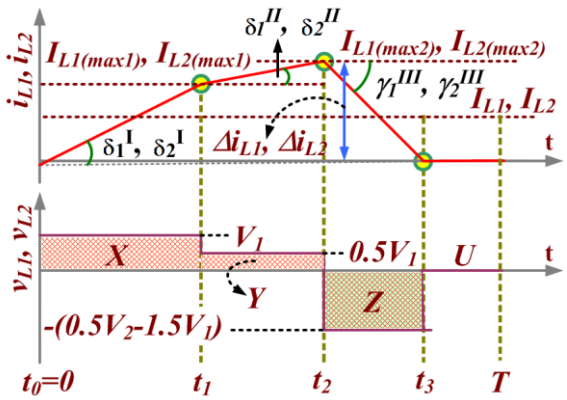

Fig. 8. Inductor voltage and current waveform.

$$\left.\begin{aligned} &I_{L1(max2)}\begin{cases}=\left(\frac{V_2-V_{C1}-V_{C2}-V_1}{2L_1}\right)k_3T\\ =\left(\frac{V_2-3V_1}{2L_1}\right)k_3T=k_3T(\gamma_1{}^{III})\end{cases}\\ &I_{L2(max2)}\begin{cases}=\left(\frac{V_2-V_{C1}-V_{C2}-V_1}{2L_2}\right)k_3T\\ =\left(\frac{V_2-3V_1}{2L_2}\right)k_3T=k_3T(\gamma_2{}^{III})\end{cases}\\ &\text{we have } L_1=L_2=L,\Rightarrow\gamma_1{}^{III}=\gamma_2{}^{III}\\ &\therefore I_{L1(max2)}=I_{L2(max2)}=I_{L(max2)} \end{aligned}\right\} t_2\le t\le t_3 \quad (12)$$

4) Mode IV [t_3-t_4]: For this mode, all the switches S_1, S_2, and S_3 are turned OFF, and inductors L_1 and L_2 currents are zero. Fig. 9 shows the equivalent circuitry of converter. It is important to note that in mode III, diode D_1 and D_2 already reversed biased when inductors and capacitors are discharged through load R. Therefore, the diode D_1 and D_2 didn't presents in the path during discharging of the inductors and capacitors and hence, diode D_1 and D_2 are not responsible for DCM. It is noteworthy that DCM occurs when diode D_o is reversed biased and all the switches are turned OFF as shown in Fig. 9.

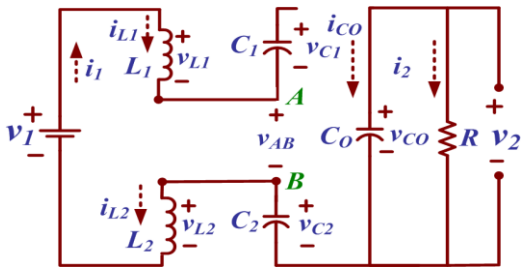

Fig. 9. DCM equivalent circuitry when all switches S_1, S_2, and S_3 are turned OFF and inductor current is zero. (Mode IV)

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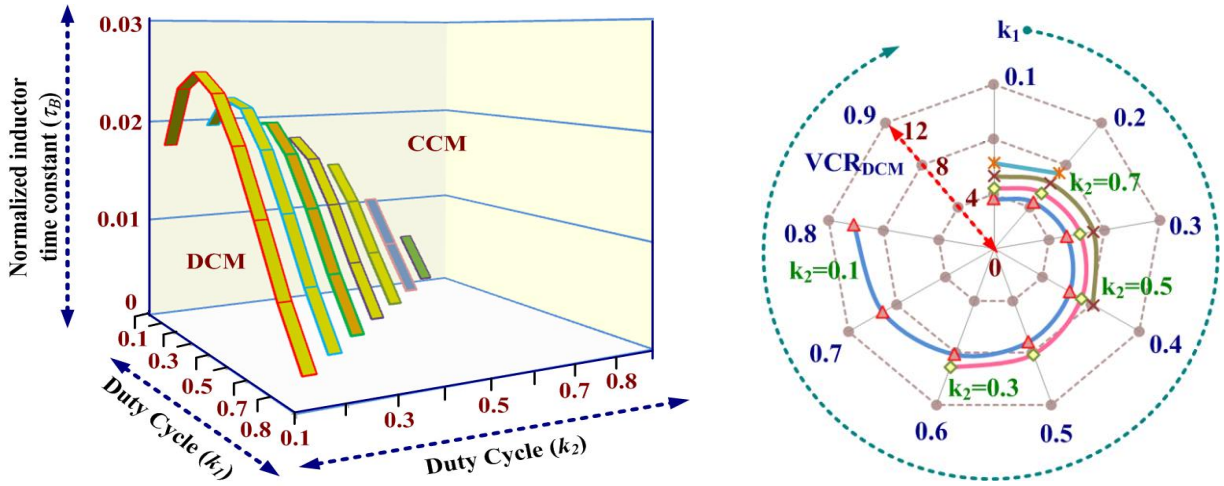

(a) (b)

Fig. 10. Curves for DCM Investigation (a) curve of normalized inductor time constant (τ_B) versus duty cycles (k_1 and k_2), (b) voltage conversion ratio (VCR_{DCM}) versus duty cycles (k_1 and k_2) at $\tau_B = 0.01$.

The energy stored in the inductors L_1 and L_2 is zero. Therefore, only energy stored in the capacitor C_o is supplied to load R. Using (11) and (12), k_3 is obtained as follows,

$$k_3 = \frac{V_1(2k_1 + k_2)}{V_2 - 3V_1} \tag{13}$$

From Fig. 7, the expression for the average capacitor C_o current is found as follows,

$$I_{Co} = \frac{I_{L1(\max 2)}k_3T - 2I_2T}{2T} = \frac{I_{L1(\max 2)}k_3T}{2T} - I_2 \tag{14}$$

Using (11)-(14), the average current of capacitor C_o is found as follows,

$$I_{Co} = \frac{\left(V_1/\sqrt{L}\right)^2(k_2+2k_1)^2T}{4(V_2-3V_1)} - \frac{V_2}{R} \tag{15}$$

Under steady state condition, the average current of capacitor is zero. Thus,

$$\frac{V_1^2(k_2+2k_1)^2T}{4L(V_2-3V_1)} = \frac{V_2}{R} \tag{16}$$

Thus, voltage conversion ratio in DCM is found as follows,

$$VCR_{DCM} = \frac{V_2}{V_1} = \frac{3}{2} + \sqrt{\frac{9}{4} + \frac{(k_2+2k_1)^2}{4\tau}}, \quad \tau = L(RT)^{-1} \tag{17}$$

Where, τ is time constant parameter which value is equal to Lf_s/R and the boundary operating condition for converter can be obtained as follows,

$$\tau_B = \frac{(k_2+2k_1)(1-k_1-k_2)^2}{4(3-k_1-2k_2)} \tag{18}$$

Where, τ_B is normalized inductor time constant at boundary. The curve of τ_B versus duty cycles is shown in Fig. 10(a). The effect of duty cycles k_1 and k_2 on voltage conversion ratio and boundary condition is analyzed and the variation in the voltage conversion ratio (VCR_{DCM}) is shown in Fig. 10(b) for τ_B=0.01 with change in duty cycle k_1 and keeping k_2 constant. The variation in the voltage conversion ratio (VCR_{DCM}) is also shown in Fig. 10(b) for τ_B=0.01 with change in duty cycle k_2 and keeping k_1 constant. If τ is smaller than τ_B, then converter operates in DCM. However, to operate the converter in CCM, following condition necessary to satisfy,

$$\tau = \frac{L}{RT} > \frac{(k_2+2k_1)(1-k_1-k_2)^2}{4(3-k_1-2k_2)} \tag{19}$$

III. Operating Behavior Under Different Inductance Values of Inductors

In this section, operating principle and behavior of the TSTM-HS converter are discussed under different inductance values of inductors. There are two cases described as follows with considering ideal semiconductor components and capacitance of the capacitors are large enough to maintain the constant voltage.

A. L_1 is Larger Than L_2 (L_1>L_2)

In this case, it is considered that the value of inductor L_1 is larger than the value of inductor L_2. Fig. 11(a) shows the inductors L_1 and L_2 current waveforms along with the switching pulses. It is notable that if the value of inductors L_1 and L_2 are equal (i.e L_1=L_2), then at any time the value of i_{L1} and i_{L2} are equal (i.e. i_{L1}=i_{L2}) and the waveform of inductor L_1 and L_2 currents are identical as discussed in section II. Nevertheless, if the values of both inductors are not same, say, the value of inductor L_1 is larger than the value of inductor L_2, then as soon as switches S_1 and S_2 are turned OFF and switch S_3 is turned ON, i_{L2} is larger than i_{L1}. Due to this, time interval PT (t_1 to t_2) shown in Fig. 11(a) is started. At this instant, inductor L_2 starts magnetizing with lower slope (nearly 0) and L_1 is still magnetizing with the same slope. When i_{L1}=i_{L2}, there is end of this time interval. Hence, in this case, there are four operating states explained as follows,

1) Mode I [t_0-t_1]:

Switches S_1 and S_2 are turned ON, and switch S_3 is turned OFF. The equivalent converter circuitry for this mode is same

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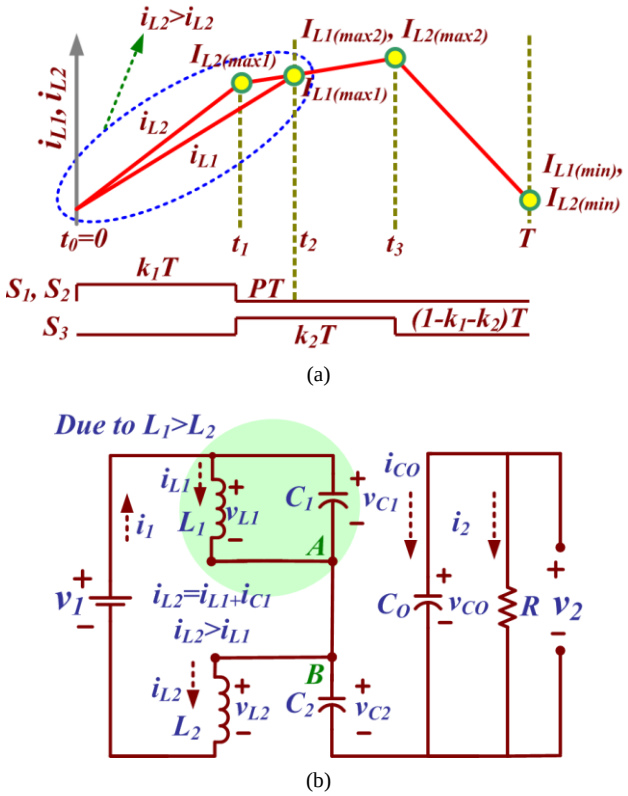

Fig. 11. When $L_1>L_2$ (a) Inductor L_1 and L_2 current waveforms along with the switching pulses, (b) equivalent circuit when switches S_1 and S_2 are turned OFF, and switch S_3 is turned ON during (t_1 to t_2) i.e. for PT time period.

as Fig. 5(a). However, the current flowing through inductor L_2 is larger than inductor L_1 i.e. ($i_{L2}>i_{L1}$). During this mode, inductors L_1, L_2, and capacitors C_1, C_2 are connected in parallel with input supply v_1. The energy stored in capacitor C_o is supplied to load R. Besides, the current through inductor L_2 is larger than the current through inductor L_1. The voltage and current equation can be obtained as follows,

$$\left.\begin{aligned} &L_1\frac{di_{L1}}{dt}=v_1,\ L_2\frac{di_{L2}}{dt}=v_1,\ Co\frac{dv_2}{dt}=\frac{-v_2}{R} \\ &i_{L1}<i_{L2} \end{aligned}\right\} t_0 \le t \le t_1 \qquad (20)$$

2) Mode II [t_1-t_2]:

Switches S_1 and S_2 are turned OFF, and switch S_3 is turned ON. Fig. 11(b) depicts the equivalent converter circuitry for this mode. During this mode, i_{L2} is larger than i_{L1}, thereby causing diode D_1 to be forward biased. Capacitor C_o is discharged into the load R. Once the current through inductors L_1 and L_2 are equal, the converter operates in mode III. The voltage and current equation can be obtained as follows,

$$\left.\begin{aligned} &L_1\frac{di_{L1}}{dt}=v_1,\ L_2\frac{di_{L2}}{dt}=v_1-V_{C1}\approx 0,\ C_o\frac{dv_2}{dt}=-\frac{v_2}{R} \\ &i_{L1}<i_{L2} \end{aligned}\right\} t_1 \le t \le t_2 \qquad (21)$$

3) Mode III [t_2-t_3]:

In this mode, switches S_1 and S_2 are still turned OFF, and switch S_3 is still turned ON. The equivalent converter circuitry for this mode is same as Fig. 5(b). In this mode, the inductors are in series and currents flowing through both the inductors are equal. Besides, C_o is still discharged into load R. Let's assume $M_1=L_1/(L_1+L_2)$ and $M_2=L_2/(L_1+L_2)$. The voltage and current equation can be obtained as follows,

$$\left.\begin{aligned} &L_1\frac{di_{L1}}{dt}=M_1v_1,\ L_2\frac{di_{L2}}{dt}=M_2v_1,\ C_o\frac{dv_2}{dt}=-\frac{v_2}{R} \\ &i_{L1}=i_{L2} \end{aligned}\right\} t_2 \le t \le t_3 \qquad (22)$$

4) Mode IV [t_3-T]:

In this mode, all switches are turned OFF. The equivalent converter circuitry for this mode is same as Fig. 5(c). During this period, both inductors L_1 and L_2, both capacitors C_1 and C_2, and input voltage v_1 are in series and provide energy to load R. The voltage and current equation can be obtained as follows,

$$\left.\begin{aligned} &L_1\frac{di_{L1}}{dt}=M_1\left(3v_1-v_2\right),\ L_2\frac{di_{L2}}{dt}=M_2\left(3v_1-v_2\right) \\ &C_o\frac{dv_2}{dt}=\frac{-v_2}{R},\ i_{L1}=i_{L2} \end{aligned}\right\} t_3 \le t \le T \qquad (23)$$

Using (21)-(23) and small approximation, the volt second balance equations for inductors can be obtained as follows,

For L_1,

$$\left.\begin{aligned} &V_1k_1T+V_1\ \ PT\ +\frac{L_1}{L_1+L_2}V_1\ \ k_2T-PT \\ &+\frac{L_1}{L_1+L_2}\frac{3V_1-V_2}{1-k_1T-k_2T} \end{aligned}\right\} = 0 \qquad (24)$$

For L_2,

$$\left.\begin{aligned} &V_1k_1T+0\ \ PT\ +\frac{L_2}{L_1+L_2}V_1\ \ k_2T-PT \\ &+\frac{L_2}{L_1+L_2}\frac{3V_1-V_2}{1-k_1T-k_2T} \end{aligned}\right\} = 0 \qquad (25)$$

Using (24) and (25), the voltage conversion ratio can be obtained as follows,

$$VCR_{CCM}\left(L_1>L_2\right)=\frac{V_2}{V_1}=\frac{3-k_1-2k_2}{1-k_1-k_2} \qquad (26)$$

It is noteworthy that the voltage conversion ratio obtained in (26) is same as (9).

B. L_2 is Larger Than L_1 ($L_2>L_1$)

In this case, it is considered that the value of inductor L_2 is larger than the value of inductor L_1. Fig. 12(a) shows the inductors L_1 and L_2 current waveforms along with the switching pulses. If the value of inductor L_2 is larger than the value of inductor L_1, then as soon as switches S_1 and S_2 are turned OFF and switch S_3 is turned ON, i_{L1} is larger than i_{L2}. Due to this, time interval PT (t_1 to t_2) shown in Fig. 12(a) is started. At this instant, inductor L_1 starts magnetizing with lower slope (nearly 0) and L_2 is still magnetizing with the same slope. When $i_{L1}=i_{L2}$, there is end of this time interval. Hence, in this case, there are four operating states explained as

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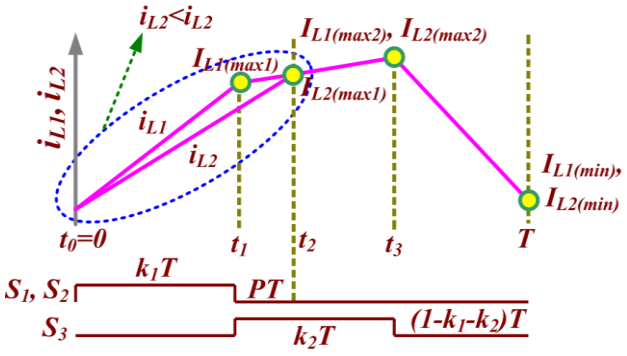
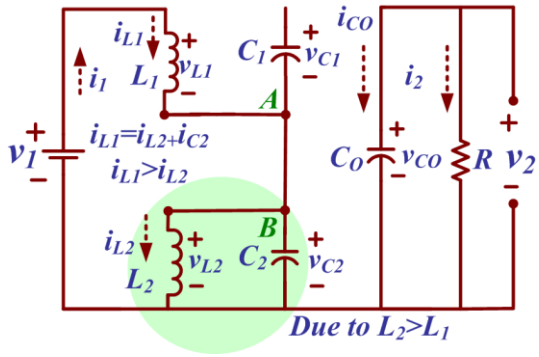


(a)



(b)

Fig. 12. When $L_1<L_2$ (a) Inductor L_1 and L_2 current waveforms along with the switching pulses, (b) equivalent circuit when switches S_1 and S_2 are turned OFF, and switch S_3 is turned ON during (t_1 to t_2) i.e. for PT time period.

follows,

1) Mode I [t_0-t_1]:

In this mode, switches S_1 and S_2 are turned ON, and switch S_3 is turned OFF. The equivalent converter circuitry for this mode is same as Fig. 5(a). However, the current flowing through inductor L_1 is larger than inductor L_2 i.e. $i_{L1}>i_{L2}$. During this mode, inductors L_1, L_2, and capacitors C_1, C_2 are connected in parallel with input supply v_1. The energy stored in capacitor C_o is supplied to load R. Besides, the current through inductor L_1 is larger than the current through inductor L_2. The voltage and current equation can be obtained as follows,

$$\left.\begin{aligned} &L_1\frac{di_{L1}}{dt}=v_1,\ L_2\frac{di_{L2}}{dt}=v_1,\ Co\frac{dv_2}{dt}=\frac{-v_2}{R} \\ &i_{L1}>i_{L2} \end{aligned}\right\} t_0 \le t \le t_1 \qquad (27)$$

2) Mode II [t_1-t_2]:

In this mode, switches S_1 and S_2 are turned OFF, and switch S_3 is turned ON. Fig. 12(b) depicts the equivalent converter circuitry for this mode. During this mode, i_{L1} is larger than i_{L2}, thereby causing diode D_2 to be forward biased. Capacitor C_o is discharged into load R. Once the current through inductor L_2 and L_1 are equal, the converter operates in mode III. The voltage and current equation can be obtained as follows,

$$\left.\begin{aligned} &L_1\frac{di_{L1}}{dt}=v_1-V_{C2}\approx 0,\ L_2\frac{di_{L2}}{dt}=V_{C2}=v_1,\ C_o\frac{dv_2}{dt}=\frac{-v_2}{R} \\ &i_{L1}>i_{L2} \end{aligned}\right\} t_1 \le t \le t_2 \qquad (28)$$

3) Mode III [t_2-t_3]:

In this mode, switches S_1 and S_2 are still turned OFF, and switch S_3 is still turned ON. The equivalent converter circuitry for this mode is same as Fig. 5(b). In this mode, the inductors L_1, L_2 are in series and current flowing through both the inductor is equal. Besides, C_o is still discharged into load R. The voltage and current equations are same as (22).

4) Mode IV [t_3-T]:

In this mode, all switches are turned OFF. The equivalent converter circuitry for this mode is same as Fig. 5(c). During this period, inductors L_1 and L_2, capacitors C_1 and C_2, and input voltage V_1 are in series and provides energy to load R. The voltage and current equation are same as (23). Using (22)-(23), (27)-(28) and small approximations, the volt second balance equations for inductors can be obtained as follows,

For L_1,

$$\left.\begin{aligned} &V_1k_1T+0\quad PT\quad +\frac{L_1}{L_1+L_2}V_1\quad k_2T-PT \\ &+\frac{L_1}{L_1+L_2}\frac{3V_1-V_2}{1-k_1T-k_2T} \end{aligned}\right\}=0 \qquad (29)$$

For L_2,

$$\left.\begin{aligned} &V_1k_1T+V_1\quad PT\quad +\frac{L_2}{L_1+L_2}V_1\quad k_2T-PT \\ &+\frac{L_2}{L_1+L_2}\frac{3V_1-V_2}{1-k_1T-k_2T} \end{aligned}\right\}=0 \qquad (30)$$

Using (29) and (30), the voltage conversion ratio can be obtained as follows,

$$VCR_{CCM}\,(L_1<L_2)=\frac{V_2}{V_1}=\frac{3-k_1-2k_2}{1-k_1-k_2} \qquad (31)$$

It is noteworthy that the voltage conversion ratio obtained in (31) is same as (9).

IV. Efficiency Analysis of TSTM-HS Converter

This section deals with the efficiency of the TSTM-HS converter. The non-idealities of inductors L_1 and L_2, input source v_1, and semiconductor devices D_1, D_2, D_o, S_1, S_2, and S_3 are considered and equivalent circuit of the TSTM-HS converter is shown in Fig. 13. The non-ideality of the voltage source is shown by considering the series resistance R_1. The non-idealities of the inductors L_1 and L_2 are shown by considering the ESR i.e. R_{L1} and R_{L2} for inductors L_1 and L_2, respectively. The non-idealities of switches S_1, S_2, and S_3 are shown by considering the ON-state resistance R_{S1}, R_{S2}, and R_{S3}, respectively. The non-idealities of diodes D_1, D_2 and D_o are shown by considering the internal resistance R_{D1}, R_{D2}, and R_{Do} and their forward voltage drop is $V_{D1\text{-}FB}$, $V_{D2\text{-}FB}$, and $V_{Do\text{-}}$

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$_{FB}$, respectively. The average current through switches S_1, S_2, and S_3 are I_{S1}, I_{S2}, and I_{S3}, respectively.

A. Mode I [t_0-t_1]

For this mode, switches S_1 and S_2 are turned ON, and switch S_3 is turned OFF. The average voltage and current of inductors and capacitors can be expressed as follows,

$$\left.\begin{aligned} &V_{L1}{}^{I}=V_1-I_1{}^{I}R_1-I_{L1}{}^{I}R_{L1}-I_{S1}{}^{I}R_{S1}\\ &V_{L2}{}^{I}=V_1-I_1{}^{I}R_1-I_{L2}{}^{I}R_{L2}-I_{S2}{}^{I}R_{S2}\\ &V_{C1}{}^{I}\approx V_1-V_{D1-FB}-I_1{}^{I}R_1-I_{D1}{}^{I}(R_{D1})-I_{S1}{}^{I}R_{S1}\\ &V_{C2}{}^{I}\approx V_1-V_{D2-FB}-I_1{}^{I}R_1-I_{D2}{}^{I}(R_{D2})-I_{S2}{}^{I}R_{S2}\\ &I_{C2}{}^{I}\approx I_1{}^{I}-I_{L1}{}^{I}-I_{L2}{}^{I}-I_{C1}{}^{I};\ I_{Co}{}^{I}\approx -V_2/R \end{aligned}\right\} \quad (32)$$

B. Mode II [t_1-t_2]

For this mode, switches S_1 and S_2 are turned OFF, and switch S_3 is turned ON. The average voltage and current for inductors and capacitors can be expressed as follows,

$$\left.\begin{aligned} &V_{L1}{}^{II}+V_{L2}{}^{II}=V_1-\left(\begin{aligned} &I_1{}^{II}R_1+I_{L1}{}^{II}R_{L1}+I_{L2}{}^{II}R_{L2}\\ &+I_1{}^{II}R_{S3}\end{aligned}\right)\\ &I_1{}^{II}=I_{L1}{}^{II}=I_{L2}{}^{II};\ I_{Co}{}^{II}\approx -V_2/R \end{aligned}\right\} \quad (33)$$

C. Mode III [t_2-t_3]:

For this mode, all switches S_1, S_2, and S_3 are turned OFF. The average amplitude of voltage and current for inductors and capacitors can be expressed as follows,

$$\left.\begin{aligned} &V_{L1}{}^{III}+V_{L2}{}^{III}=V_1-V_2-\left(\begin{aligned} &I_1{}^{III}R_1+I_{L1}{}^{III}R_{L1}+I_{L2}{}^{III}R_{L2}\\ &+I_1{}^{III}R_{Do}+V_{Do-FB}\end{aligned}\right)\\ &I_1{}^{III}=I_{L1}{}^{III}=I_{L2}{}^{III};\ I_{Co}{}^{III}\approx I_1-V_2/R \end{aligned}\right\} \quad (34)$$

Due to identical inductors (i.e. L_1=L_2=L), the ESR of both inductors L_1 and L_2 are same, that means R_{L1}=R_{L2}=R_L. Due to identical switches S_1 and S_2 (*i.e.* S_1=S_2=S), the ON-state resistance of switches are same, that means R_{S1}=R_{S2}=R_S. Due to identical diodes D_1, D_2, and D_o (i.e D_1=D_2=D_o=D), the internal resistance and forward voltage drop for diodes are same, that means R_{D1}=R_{D2}=R_{Do}=R_D and $V_{D1\text{-}FB}$=$V_{D2\text{-}FB}$=$V_{Do\text{-}FB}$=V_D. As a result, following equations are obtained by using (32)-(34).

$$\left.\begin{aligned} &V_L{}^{I}=V_{L1}{}^{I}=V_{L2}{}^{I}\approx V_1-I_1{}^{I}R_1-I_L{}^{I}(R_S+R_L)\\ &V_{C1}{}^{I}\approx V_{C2}{}^{I}\approx V_1-V_{D-FB}-I_1{}^{I}R_1-I_D{}^{I}(R_D)-I_L{}^{I}R_S\\ &I_{Co}{}^{I}\approx -V_2/R \end{aligned}\right\} \quad (35)$$

$$\left.\begin{aligned} &V_L{}^{II}=V_{L1}{}^{II}=V_{L2}{}^{II}\approx V_1-I_1{}^{I}(R_1+2R_L+R_S)\\ &I_{Co}{}^{II}\approx -V_2/R \end{aligned}\right\} \quad (36)$$

$$\left.\begin{aligned} &V_L{}^{III}=V_{L1}{}^{III}=V_{L2}{}^{III}\approx\frac{V_1-V_2-\left(I_1{}^{III}(R_1+2R_L+R_D)+V_{D-FB}\right)}{2}\\ &I_{Co}{}^{III}=I_{L1}{}^{III}-V_2/R=I_{L2}{}^{III}-V_2/R=I_1{}^{III}-V_2/R\\ &I_1{}^{III}=I_{L1}{}^{III}=I_{L2}{}^{III} \end{aligned}\right\} \quad (37)$$

Using capacitor charged-balance method, inductors L_1 and L_2 currents are obtained as follows,

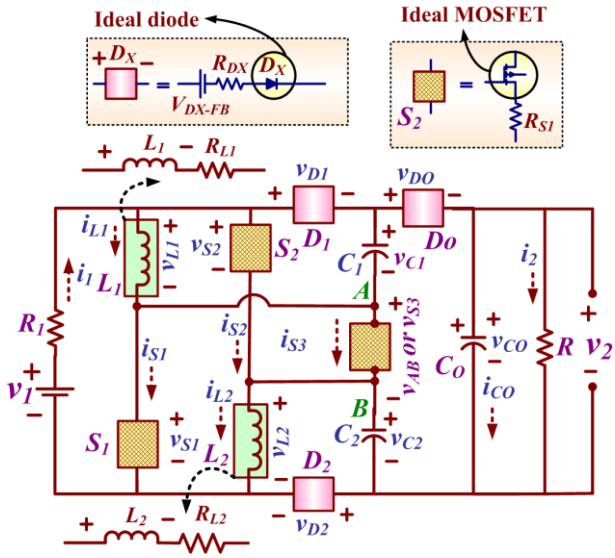

Fig. 13. Power circuitry of TSTM-HS converter with non-idealities.

$$\left.\begin{aligned} &\int_0^{k_1T}\left(I_{Co}{}^{I}\right)dt+\int_0^{k_2T}\left(I_{Co}{}^{II}\right)dt+\int_0^{T-k_1T-k_2T}\left(I_{Co}{}^{III}\right)dt=0\\ &I_L=I_{L1}=I_{L2}=\frac{V_2}{R}(1-k_1-k_2)^{-1} \end{aligned}\right\} \quad (38)$$

Using inductor-volt-second-balance method on inductors L_1 or L_2, the voltage conversion ratio is obtained as follows,

$$\left.\begin{aligned} &\int_0^{k_1T}\left(V_L{}^{I}\right)dt+\int_0^{k_2T}\left(V_L{}^{II}\right)dt+\int_0^{T-k_1T-k_2T}\left(V_L{}^{III}\right)dt=0\\ &VCR_{CCM}=\frac{V_2}{V_1}=\frac{\left\{(1+k_1)-\frac{V_D}{V_1}(1-k_1-k_2)\right\}}{\left\{\begin{aligned}&2R_Sk_1+R_Sk_2\\&+2R_L\\&+\frac{R_D(1+k_1-K_2)}{R(1-k_1-k_2)}\end{aligned}\right\}+(1-k_1-k_2)}+\frac{V_{C1}+V_{C2}}{V_1} \end{aligned}\right\} \quad (39)$$

Where, V_{C1}/V_1 and V_{C2}/V_1 is

$$\left\{\begin{aligned} &\frac{V_{C1}}{V_1}\approx 1-\frac{I_1R_1+V_D+I_{D1}(R_D)+I_{S1}R_S}{V_1}\\ &\frac{V_{C2}}{V_1}\approx 1-\frac{I_1R_1+V_D+I_{D2}(R_D)+I_{S2}R_S}{V_1}\\ &I_1R_1=\text{voltage drop across resistance } R_1\\ &V_D+I_{D1}(R_D)=\text{voltage drop across diode } D_1\\ &V_D+I_{D2}(R_D)=\text{voltage drop across diode } D_2\\ &I_{S1}R_S,\ I_{S2}R_S=\text{voltage drop across switch } S_1,\ S_2 \end{aligned}\right.$$

Therefore, the voltage conversion ratio of the TSTM converter is restricted by internal resistance R_L, R_S, V_D, and R_D. For e.g. if R_L=300m**Ω**, R_S=200m**Ω**, V_D=0.8V, R_D=0.01**Ω**, and R_L=320**Ω**, then at k_1=50% and k_2=35%, then practical voltage conversion ratio is 10.89. However, if all the components are ideal then the voltage conversion ratio is 12.

Switching losses of the switches is P_{SW} and can be obtained as follows,

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$$P_{SW} = P_{SW1} + P_{SW2} + P_{SW3} = \begin{pmatrix} V_{S1}I_{S1}(t_{r1}+t_{f1})f \\ +V_{S2}I_{S2}(t_{r2}+t_{f2})f \\ +V_{S3}I_{S3}(t_{r3}+t_{f3})f \end{pmatrix} \quad (40)$$

Where t_{r1}, t_{r2}, t_{r3} and t_{f1}, t_{f2}, t_{f3} are the rising and falling time for the switches S_1, S_2, and S_3, respectively and f is switching frequency. The average voltage across switches S_1, S_2, and S_3, are V_{S1}, V_{S2}, and V_{S3}, respectively. The total input power P_1 and output power P_2 are obtained as follows,

$$\left.\begin{aligned} P_1 &= V_1\begin{pmatrix} I_{L1}k_1+I_{L2}k_1+I_{C1}k_1+I_{C2}k_1+\frac{1}{2}I_{L1}k_2 \\ +\frac{1}{2}I_{L2}k_2+I_L(1-k_1-k_2) \end{pmatrix} + P_{SW} \\ P_1 &= \frac{V_1V_2}{R}\left(1+k_1\right)\left(1-k_1-k_2\right)^{-1} + 2V_1I_{C1}k_1 + P_{SW} \\ P_2 &= V_2I_2 = V_2^{\,2}/R \end{aligned}\right\} \quad (41)$$

Using (39) and (41), efficiency of the TSTM-HS converter is obtained as,

$$\eta\left\{\begin{aligned} &= \frac{V_2/V_1}{(1+k_1)(1-k_1-k_2)^{-1}+2V_1I_{C1}k_1+P_{SW}} \\ &= \frac{V_2/V_1}{(1+k_1)(1-k_1-k_2)^{-1}+4\pi fV_1^{\,2}C_1k_1+P_{SW}} \end{aligned}\right. \quad (42)$$

V. Design and Comparison

To design the TSTM-HS converter, necessary parameters are typical supply voltage (V_1), nominal output voltage (V_2), required output current (I_2) to drive the load, switching frequency (f), and load (R).

A. Selection of Duty cycles

For simplicity, the voltage conversion ratio of TSTM-HS converter is written similar to conventional boost converter as follows,

$$\left.\begin{aligned} VCR_{CCM} &= \frac{3-k_1-2k_2}{1-k_1-k_2} = \frac{1}{1-K_{TSTM-HS}(k_1,k_2)} \\ K_{TSTM-HS}(k_1,k_2) &= \left(2-k_2\right)/\left(3-k_1-2k_2\right) \end{aligned}\right\} \quad (43)$$

Where $K_{TSTM\text{-}HS}(k_1, k_2)$ is function of duty cycles k_1 and k_2. Initially, the function of duty cycles $K_{TSTM\text{-}HS}(k_1, k_2)$ is selected as follows,

$$K_{TSTM-HS}(k_1,k_2)=1-\frac{V_1}{V_2}\eta\Big\} \quad (44)$$

For superior design, the worst case of efficiency is considered while calculating the function of duty cycles. As a result, calculation provides a more practical value of function of duty cycles. It is noticeable that the worst efficiency of TSTM-HS configuration is expected 85%.

B. Design of Inductors (L_1 and L_2)

Based on the functionality, it is possible to select both inductors with equal inductance rating i.e. L_1=L_2=L. Therefore, the ripple in both the inductors are same i.e. Δi_{L1} = Δi_{L2} =Δi_L. The design of the inductor L is dependent on the switching frequency (f), typical input voltage (V_1), duty cycles (k_1 and k_2), and ripple current $\Delta i_{L(max2\text{-}min)}$. The good estimation of value of $\Delta i_{L(max2\text{-}min)}$ *or* Δi_L is in between 20% to 40% of inductor L_1 and L_2 current and can be obtained as follows,

$$\Delta i_{L(\max 2\text{-}\min)} = I_{L(max2)} - I_{L(min)} = 20 \text{ to } 40\% \text{ of } \Delta i_L \quad (45)$$

The critical inductance (L_{cric}) is calculated as follows,

$$L_{cric} = \frac{k_1V_1+k_2(V_1/2)}{f\times\Delta i_{L(\max 2\text{-}\min)}} = \frac{k_1V_1+k_2(V_1/2)}{f\times\Delta i_L} \quad (46)$$

For good design, the inductors L_1 and L_2 current ripple should be considered 20% of average current of inductors I_{L1} and I_{L2}, respectively. In order to operate converter in CCM, the inductance of inductors L_1 and L_2 must be greater than L_{cric}. The current rating of the inductors (I_{L1}=I_{L2}=I_L) can be decided as follows,

$$I_L > I_1 + \frac{\Delta i_{L(\max 2\text{-}\min)}}{2} = \begin{pmatrix} \frac{V_2}{R(1-K_{TSTM-HS}(k_1,k_2))} \\ +\frac{\Delta i_{L(\max 2\text{-}\min)}}{2} \end{pmatrix} \quad (47)$$

C. Design of Intermediate Capacitors (C_1 and C_2)

Capacitors C_1 and C_2 design is dependent on the input voltage, duty cycle (k_1), and voltage ripples (ΔV_{C1} and ΔV_{C2}). For good design, it is considered that the voltage ripple in the capacitors C_1 and C_2 voltage is 1% of the total input voltage. Based on the functionality of converter, it is possible to select both capacitors C_1 and C_2 with equal capacitance rating i.e. C_1=C_2. The voltage rating and critical capacitance for both the capacitors C_1 and C_2 are calculated as follows,

$$\left.\begin{aligned} C_{C1,cric} \text{ or } C_{C2,cric} &= \frac{k_1(I_1-2I_L)}{2\times f\times\Delta V_C} \\ V_{C1} \text{ or } V_{C2} &\geq V_1+\Delta V_1 > V_1 \end{aligned}\right\} \quad (48)$$

D. Design of Output Capacitor (C_o)

The design of the capacitor C_o is dependent on the output voltage (V_2), output power (P_o) or load (R), duty cycle (k_1, k_2) switching frequency (f), and output voltage ripples (ΔV_{Co}). For good design, it is considered that the voltage ripple across capacitor C_o is 1% of the output voltage. The voltage rating and critical capacitance for capacitors C_o are calculated as follows,

$$\left.\begin{aligned} C_{o,cric} &= \frac{(k_1+k_2)P_2}{V_2\times f\times\Delta V_{Co}} = \frac{(k_1+k_2)V_2}{R\times f\times 1\% \text{ of } V_2} \\ VC_o &\geq V_2+\Delta V_2 > V_2 \end{aligned}\right\} \quad (49)$$

E. Selection of Semiconductor Devices

The blocking voltages of switches S_1, S_2, and S_o are analyzed in each mode and given as follows,

$$V_{S1} = V_{S2}\begin{cases} =0 \ Mode-I \\ =\frac{V_1}{2} Mode-II \\ =\frac{(V_2-V_1)}{2} Mode-III \end{cases} ; V_{S3} = \begin{cases} =-V_1 \ Mode-I \\ =0 \ Mode-II \\ =V_2-2V_1 \ Mode-III \end{cases} \quad (50)$$

The voltage ratings of the switches S_1, S_2, and S_o are

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calculated as follows,

$$(V_{S1}=V_{S1}) > \frac{V_1}{2}\left(\frac{2-k_2}{1-k_1-k_2}\right); V_{S3} > V_1\left(\frac{1+k_1}{1-k_1-k_2}\right) \quad (51)$$

The voltages across diodes D_1, D_2, and D_o are analyzed in each mode and given as follows,

$$V_{D1}\begin{cases} = 0\ Mode-I \\ = \frac{-V_1}{2} Mode-II \\ = \frac{-(V_2-V_1)}{2}\ Mode-III \end{cases}; V_{D0}\begin{cases} = -(V_2-V_1)\ Mode-I \\ = -(V_2-2V_1)\ Mode-II \\ = 0\ Mode-III \end{cases} \quad (52)$$

The Peak Inverse Voltage (PIV) of the diodes D_1, D_2, and D_o is expressed as follows,

$$\left.\begin{aligned} PIV\ \text{of}\ V_{D1}\ or\ V_{D2} &\geq \frac{V_1}{2}\left(\frac{2-k_2}{1-k_1-k_2}\right) \\ PIV\ \text{of}\ V_{D0} &\geq V_1\left(\frac{2-k_2}{1-k_1-k_2}\right) \end{aligned}\right\} \quad (53)$$

It is suggested that the voltage rating of diodes must be greater than PIV values.

F. Comparison of Converters

The proposed TSTM-HS converter is compared with recently addressed converters in terms of number of components, voltage conversion ratio, and voltage stress. The detail comparison is tabulated in Table-I. It is notable that the voltage conversion ratio of conventional boost, switched inductor boost converter [23], ZETA derived converter [24], and SEPIC derived converter [24] are controlled through single switch. To increase the voltage conversion ratio, switched inductor network and diode-capacitor circuitry is employed in [24]. Nevertheless, the voltage conversion ratio is not significantly improved even though using multiple capacitors in ZETA/SEPIC derived converters and inductors in switched inductor boost converter. Furthermore, three different converter configurations (Converter –I, II, and III) are proposed with two switches [23]. However, both the switches of converter-I, II, and III are operate simultaneously and the voltage conversion ratio of converter-I, II and III are not high even though using two switches and two inductors. Moreover, the operating principle of conventional converter and the suggested converters in [23]-[24] are dependent on single duty cycle and it is not possible to operate at wide duty cycle range. In [25], two inductors, three switches and two different duty cycles are used to achieve higher conversion ratio. However, the voltage rating of devices restricts the voltage conversion ratio. Also, the conversion ratio is not significantly increase though using three switches. The TSTM-HS converter provides high voltage conversion ratio with wide duty range and reduced voltage stress on components. Theoretically, compared to the proposed converter, quadratic boost converter (QBC) [13], [18] provides higher voltage gain. However, in QBC, the voltage conversion ratio is dependent on single duty. Moreover, there is non-linear relationship between input and output voltage of QBC due to high conversion ratio. Hence, small change in duty cycle will change output voltage by large values. Therefore, more complex control is required to control the switch. The main benefits of the TSTM-HS configuration is the operating range is increased by operating converter in three modes with double duty ratio. Hence, the converter can be operated at higher duty ratio (sum of two duty ratios). Moreover, the energy is transferred without multiple energy transfer loops which increases the efficiency and performance. Moreover, the output voltage of proposed converter is based on the two duty ratios k_1 and k_2. Owing to the advantages of two duty ratios, when the voltage changed the operation of proposed converter can be controlled in three possible ways 1) fixed duty ratio k_1 and variation in duty ratio k_2, 2) variation in duty ratio k_1 and fixed duty ratio k_2, and 3) variation in both duty ratios k_1 and k_2. Additional advantages could be a scenario in that one may use one duty ratio for MPPT tracking and another to control output voltage. The TSTM-HS provide a reliable operation with wide duty range and flexibility to control conversion ratio by adjusting two different duty cycles

TABLE I. COMPARISON OF TSTM-HS CONVERTER WITH RECENTLY PROPOSED CONVERTERS

	V_2/V_1	Intermediate Capacitor voltage rating	PIV of diode		Max. Switch Voltage	Number of	Approx. Cost of Power Circuit
			Load side diodes	Intermediate diodes		N_I/ N_C/ N_S/ N_D	
A	$1/(1-k)$	-	$-V_2$	-	V_2	1/ 1/ 1/ 1	$C_L+C_C+C_S+C_D+EC$
B	$(1+k)/(1-k)$	-	$-V_2$,	$-V_1$, $-(V_2-V_1)/2$	V_2	2/ 1/ 1/ 4	$2C_L+1C_C+1C_S+4C_D+EC$
C	$(1+k)/(1-k)$	$(V_2-V_1)/2$	$-(V_2+V_1)/2$	-	$V_2/(1+k)$	1/ 3/ 1/ 3	$1C_L+3C_C+1C_S+3C_D+EC$
D	$(2-k)/(1-k)$	V_1	$-(V_2-V_1)$	-	$V_2/(2-k)$	2/ 4/ 1/ 3	$2C_L+4C_C+1C_S+3C_D+EC$
E	$(1+k)/(1-k)$	-	$-(V_2+V_1)$	$-(V_2+V_1)/2$	$(V_2+V_1)/2$	2/ 1/ 2/ 1	$2C_L+1C_C+2C_S+1C_D+EC$
F	$2/(1-k)$	V_1	$-V_2$	$-V_2/2$	$V_2/2$	2/ 2/ 2/ 2	$2C_L+2C_C+2C_S+2C_D+EC$
G	$(3-k)/(1-k)$	V_1	$-(V_2-V_1)$,	$-(V_2-V_1)/2$	$(V_2-V_1)/2$	2/ 3/2/ 3	$2C_L+3C_C+2C_S+3C_D+EC$
H	$(1-k_1)/(1-k_1-k_2)$	-	$-V_2$	$-V_1$	$(V_2+V_1)/2$, V_2	2/ 1/ 3/ 2	$2C_L+1C_C+3C_S+2C_D+EC$
I	$1/(1-k)^2$	$V_2(1-k)$	$-V_2$	$-V_2(1-k)$	V_2	2/2/1/3	$2C_L+2C_C+1C_S+3C_D+EC$
J	$(3-k_1-2k_2)/(1-k_1-k_2)$	V_1	$-(V_2-V_1)/2$	$-(V_2-V_1)$	$(V_2-V_1)/2$, V_2-2V_1	2/ 3/ 3/3	$2C_L+3C_C+3C_S+3C_D+EC$

Note-A: Boost Converter, B: Switched Inductor Boost Converter [23], C: ZETA Derived Converter [24], D: SEPIC Derived Converter [24], E: Converter-I [23], F: Converter-II [23], G: Converter-III [23], H: High Gain Converter [25], I: Quadratic Boost Converter [13], [18], J: Proposed Converter, N_I: Number of inductors, N_C: Number of Capacitors, N_S: Number of switches, N_D: Number of diodes, C_L: Cost of single inductor, C_C: Cost of single capacitor, C_S: Cost of single switch, C_D: Cost of single diodes, EC: Extra cost.

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which is not possible from any single switch converters. Moreover, it is observed that the voltage stress of semiconductor devices are low in proposed converter compared to recently proposed converter [23]-[25]. Therefore, low voltage rating devices with low internal resistance can be used to design proposed converter.

VI. Experimental Results and Discussion

The theoretical analysis of TSTM-HS converter is validated through experimental investigations in the laboratory. The TSTM-HS converter is designed according to abovementioned designed procedure with load power (P_2) 500W, input voltage (v_1) 36V, and output voltage (v_2) 400V. To design the prototype, two identical ferrite core type inductors (L_1 and L_2) are selected with inductance 100µH, current capability 20A, and internal series resistance 300mΩ (for design, it is assumed that inductor ripples Δi_L is 40% of inductor L_1 and L_2 current). The two identical capacitors C_1 and C_2 (100µF/50V, ESR=0.05Ω) along with two identical diodes D_1 and D_2 (STTH30R04) are used at the intermediate stages whose forward voltage drop V_D is 0.8V and ON-state resistance R_D is 0.01Ω. At the load side, diodes D_o (STTH30R04) and capacitor C_o (100µF/450V, ESR=0.07Ω) are used. The semiconductor control switches FDP19N40 (ON-state resistance R_S=200mΩ) are used along with flat-type heat sink and gate pulses are generated through FPGA. The two gate pulses are generated with 50% duty cycle (k_1) to control switches S_1 and S_2. Also, the gate pulse with 35% duty cycle is generated to control switch S_3. The converter is operated at switching frequency 50kHz.

In Fig. 14(a), it is observed that the output voltage (V_2) 401.1V is generated from the input voltage (V_1) 36.3V. In the beginning of mode I (A_1 in Fig. 14(a)), spike of 9.38A is observed in the input current due to charging of capacitors C_1 and C_2. The sudden current fall is observed in the input current (B_1 in Fig. 14(a)) when converter operation is changed from mode I to mode II, which is expected according to operation. During mode III, the slope of input current is negative. The average load current (I_2) and input current (I_1) is 1.26A and 14.9A, respectively. In Fig. 14(b), it is observed that the slope of currents i_{L1} and i_{l2} are positive during mode I and II. Hence, both inductors L_1 and L_2 are charging. The slope of the currents i_{L1} and i_{l2} are exactly half in mode II compared to slope in mode I as expected. During mode III, the slope of currents i_{L1} and i_{l2} is negative. Hence, both the inductors L_1 and L_2 are discharging. The practically observed average value of output voltage (v_2), inductor L_1 current (i_{L1}), inductor L_2 current (i_{l2}), and input current (i_1) is 401.1V, 8.56A, 8.53A, and 14.9A, respectively. In Fig. 14(c), it is observed that both inductors L_1 and L_2 are charged in parallel during mode I and voltage across each inductor is equal to input voltage (V_1) 36.3V. In mode II, both inductors L_1 and L_2 are charged in series with input voltage 36.3V. Also, in mode II, little fluctuations are observed in the voltages v_{L1} and v_{L2} as shown by A_1 and B_1 in Fig. 14(c), respectively due to little practical difference in the inductance of L_1 and L_2. During mode III, both inductors L_1 and L_2 are discharged through load and the voltage across each inductor is 146.3V. Also, due to switching, little transients are observed in the voltages v_{L1} and

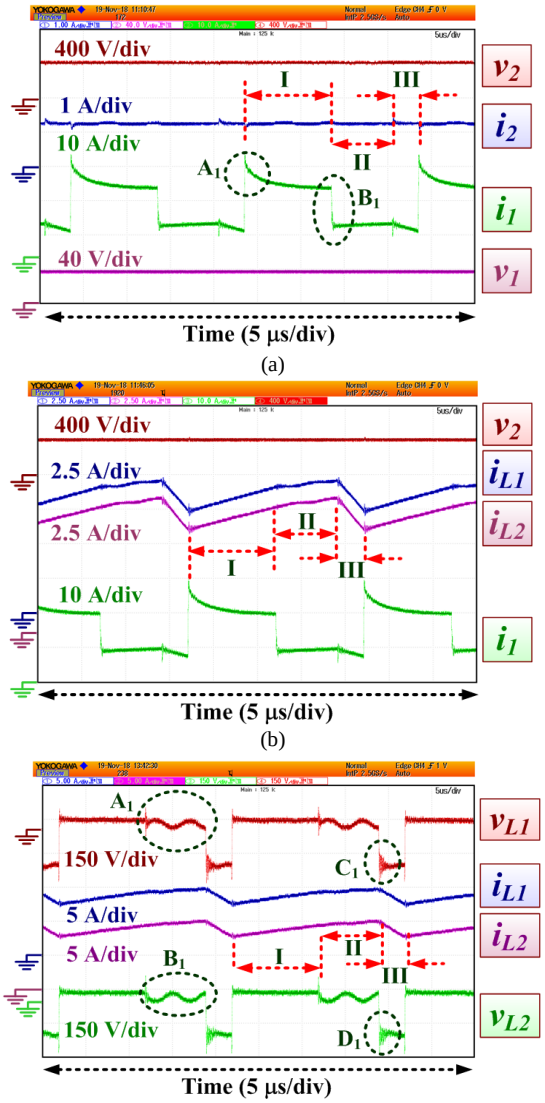

Fig. 14. Experimental results of TSTM-HS converter, (a) top to bottom: output voltage (v_2), output current (i_2), input current (i_1), and input voltage (v_1), (b) top to bottom: output voltage (v_2), inductor L_1 current (i_{L1}), inductor L_2 current (i_{l2}), and input current (i_1), and (c) top to bottom: inductor L_1 voltage (v_{L1}), inductor L_1 current (i_{L1}), inductor L_2 current (i_{L2}), and inductor L_2 voltage (v_{L2}).

v_{L2} as shown by C_1 and D_1 in Fig. 14(c), respectively. The practically observed average value of inductor L_1 voltage (v_{L1}), inductor L_1 current (i_{L1}), inductor L_2 voltage (v_{L2}), and inductor L_2 current (i_{L2}) is 0.72V, 8.56A, 0.59V, 8.53 A, respectively.

In Fig. 15(a), during mode I, the switch S_2 is conducting and the voltage across nodes A-B is equal to $-V_1$ and observed value is 36.1V. During Mode II, little fluctuations are observed across switch S_2. However, the expected average voltage across switch S_2 is $(V_1/2)$ and observed value is 18.3V. During mode III, the expected average voltage across nodes A-B is equal to $V_2 - 2V_1$ and observed value is 328.1V. In Mode III, little fluctuations are observed across switch S_2. However, the expected average voltage across switch S_2 is $(V_2 - V_1)/2$ and observed value is 183.3V. In Fig. 15(b), during mode I, diode D_1 is conducting, the expected voltage across diode D_o is $-(V_2-V_1)$ and observed value is -364.6V. During Mode II, diodes D_o and D_1 are reversed biased and little

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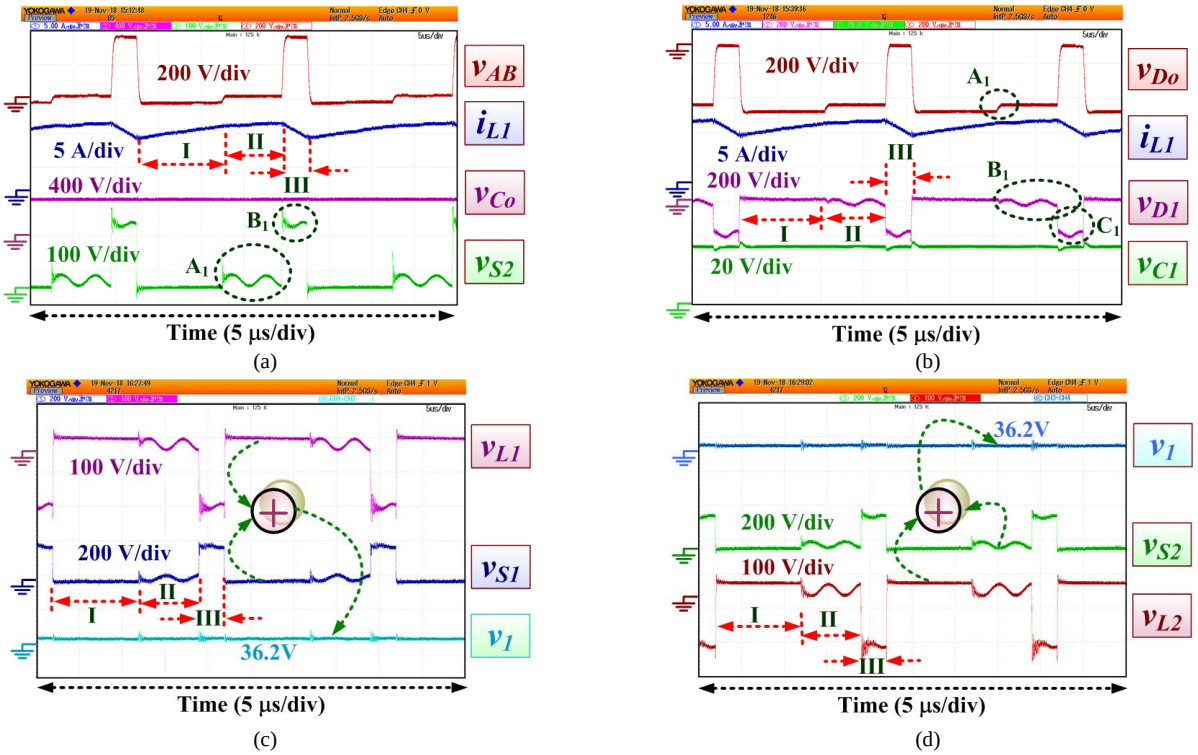

Fig. 15. Experimental results of TSTM-HS converter, (a) top to bottom: voltage across nodes A-B (v_{AB}), inductor L_1 current (i_{L1}), capacitor C_o voltage (v_{Co}), and voltage across switch S_2 (v_{S2}) (b) top to bottom: voltage across diode D_o (v_{Do}), inductor L_1 current (i_{L1}), voltage across diode D_1 (v_{D1}), and capacitor C_1 voltage (v_{C1}), (c) top to bottom: inductor L_1 voltage (v_{L1}), voltage across switch S_1 (v_{S1}), and resultant of (v_{L1}+ v_{S1}), (d) bottom to top: inductor L_2 voltage (v_{L2}), voltage across switch S_2 (v_{S2}), and resultant of (v_{L2}+ v_{S2}).

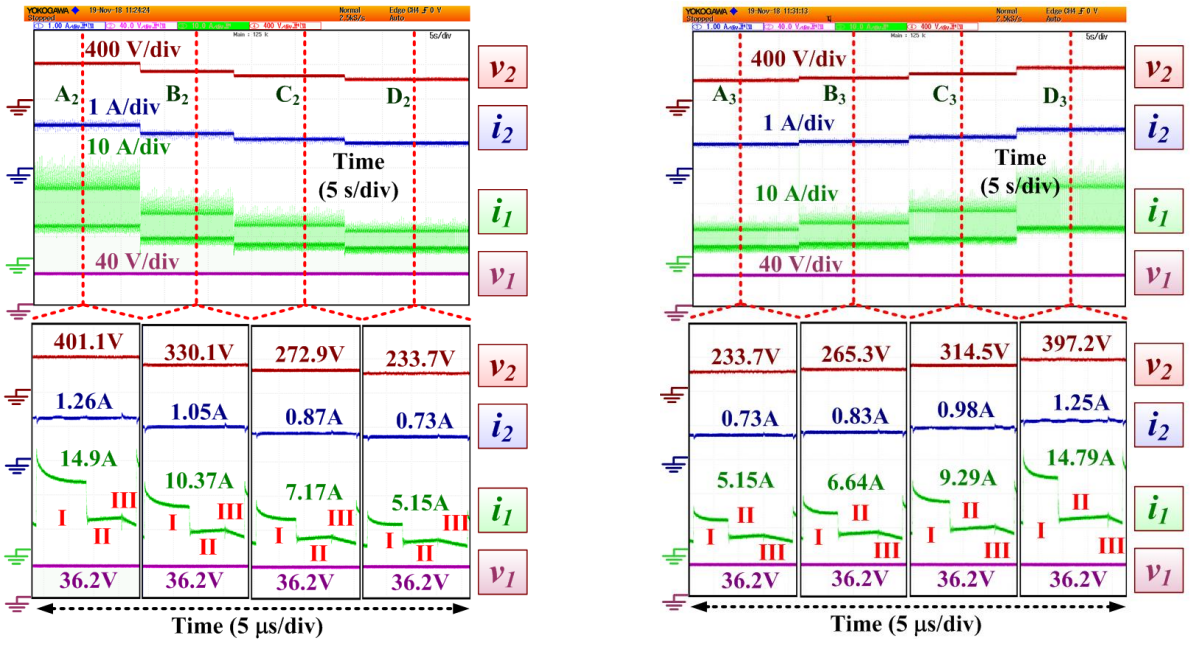

Fig. 16. Experimental results of TSTM-HS converter at different power levels and variation in duty cycles (a) output voltage (v_2), output current (i_2), input voltage (v_1), and input current (i_1) where, duty cycle k_1 is regulated from 50% to 35% and duty cycle k_2 is constant 35%, (b) output voltage (v_2), output current (i_2), input voltage (v_1), and input current (i_1) where, duty cycle k_1 is constant 35% and the duty cycle k_2 is regulated from 35% to 50%.

fluctuations across voltage across D_1 is observed. However, the average voltage across diodes D_o and D_1 is -328.1V and -18.7V, respectively. During mode III, the diode D_o is conducting and the average voltage across diode D_1 and capacitor C_1 (V_{C1}) is -183.1V and 35.7V, respectively. In Fig. 15(c), it is clearly observed that the addition of the average inductor L_1 voltage (v_{L1}) and average voltage across switch S_1 (v_{S1}) is 36.2V which is equal to the magnitude of input voltage. In Fig. 15(d), it is clearly observed that the addition of the average inductor L_2 voltage (v_{L2}) and average voltage

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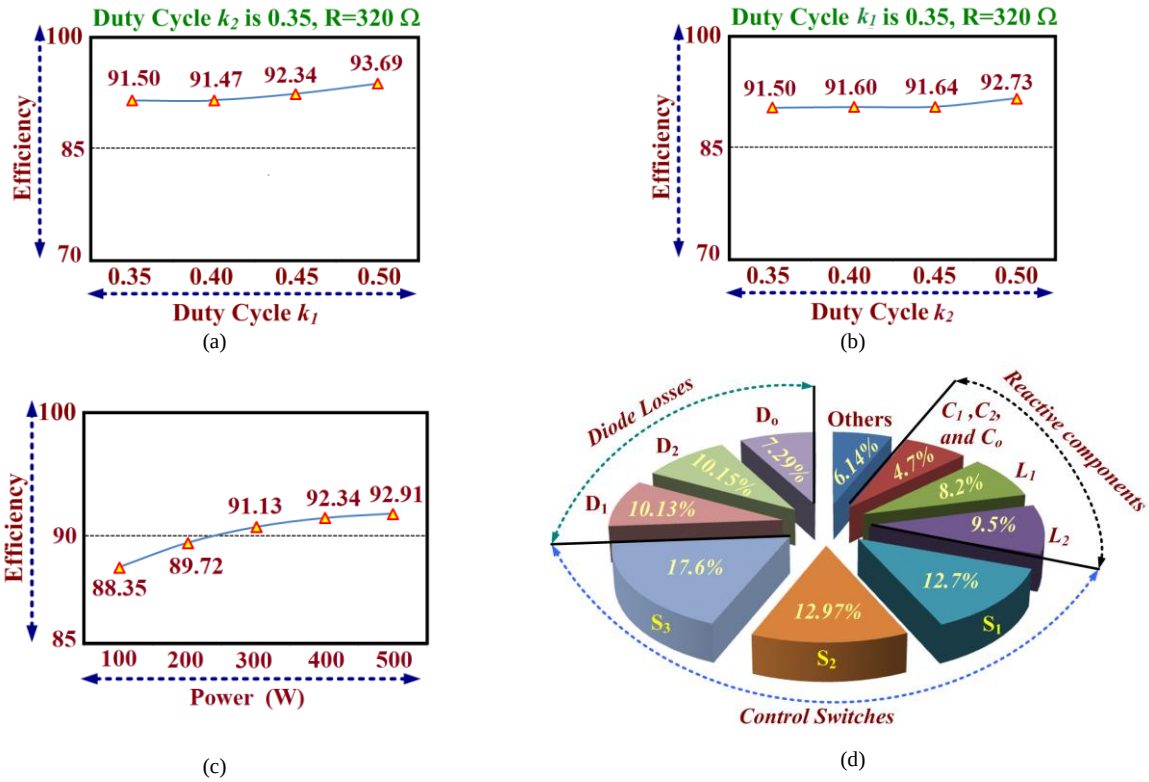

Fig. 17. Experimental Efficiency curves (a) efficiency versus duty cycle k_1, (b) efficiency versus duty cycle k_2, (c) efficiency versus power, (d) Loss distribution.

across switch S_2 (v_{S2}) is 36.2V which is equal to the magnitude of input voltage. To investigate the effect of duty cycles on the voltage regulation of the converter, the circuitry is tested in open loop with the perturbation in duty cycles. The performance is investigated with constant input voltage 36.2V and load R=320Ω. Fig. 16(a) show the waveform of output voltage (v_2), output current (i_2), input voltage (v_1), and input current (i_1) where, duty cycle k_1 is regulated from 50% to 35% (with the interval of 5%) and duty cycle k_2 is constant 35%. It is observed that the output voltage is decreases when duty cycle k_1 is reduced and duty cycle k_2 is constant. The voltage conversion ratio of converter is reduced when width of the mode I is reduced without changing the width for mode II, which is clearly observed by the values given in Fig. 16(a). Fig. 16(b) show the waveform of output voltage (v_2), output current (i_2), input voltage (v_1), and input current (i_1) where, duty cycle k_1 is constant 35% and the duty cycle k_2 is regulated from 35% to 50% (with the interval of 5%). It is observed that the output voltage is increases when duty cycle k_2 is increases and duty cycle k_1 is constant. The voltage conversion ratio of converter is increased when width of the mode II is increased without changing the width for mode I, which is clearly observed by the values given in Fig. 16(b). Fig. 17(a) shows the plot of efficiency versus duty cycle k_1 with constant load 320Ω and duty cycle k_2=35%. Fig. 17(b) shows the plot of efficiency versus duty cycle k_2 with constant load 320Ω and duty cycle k_1=35%. The efficiency versus power plot is shown in Fig. 17(c). At power 100W and 500W, the experimentally observed efficiency of the converter is 88.35% and 92.91%, respectively. It is noteworthy that based on the several test the average efficiency of the proposed converter is 92.06%. The loss distribution for each component of designed converter is shown in Fig. 17(d). It is observed that the 22.4%, 43.27%, 27.15%, and 6.14% losses occurs due to reactive components, control switches, diodes, and other parts of converter, respectively. The experimental investigation shows the good agreement with theoretical analysis. Based on the investigation, it can be conclude that the proposed converter circuitry is suitable for DC microgrid application.

VII. Conclusion

A new Triple-Switch-Triple-Mode High Step-up (TSTM-HS) DC-DC converter is proposed with wide range of duty cycle. The voltage conversion ratio is adjusted by two different duty cycles and operates in three modes to achieve high conversion ratio without using high duty cycle for individual switch. The CCM, DCM characteristics waveform are analyzed and CCM-DCM boundary is explained in detail. The efficiency and comparison is provided and it is notable that the proposed converter provides high voltage conversion ratio with reduce voltage stress across diodes and switches. Therefore, the proposed TSTM-HS converter provides a viable solution for low DC to high DC conversion in DC microgrid application. The effect of two duty cycles on voltage conversion ratio is studied in detail and it can be conclude that the proposed converter provides a high voltage conversion ratio with wide duty range which is not possible by any singe switch DC-DC converter. The experimental results confirm the theoretical analysis, feasibility, and performance of the proposed TSTM-HS converter.

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